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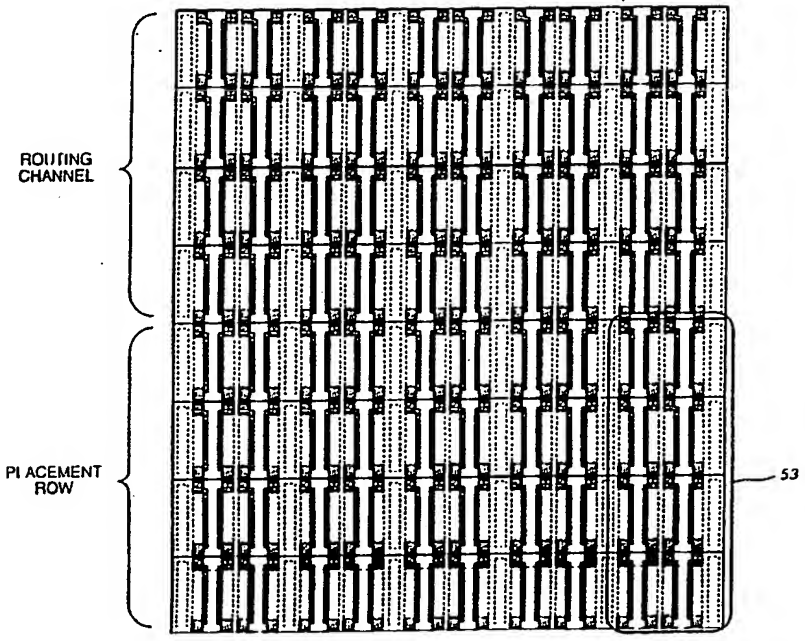


(57) Abstract

A gate array placement row includes three or more transistor rows, with each transistor row containing multiple transistors all of a given type while alternate transistor rows contain transistors of opposite types. Each transistor row is five or more routing tracks high in the column direction.

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# GATE ARRAY BASES WITH FLEXIBLE ROUTING

## BACKGROUND OF THE INVENTION

### Field of the Invention:

The present invention generally relates to gate array circuits, and, more particularly, the present invention relates to large semi-custom integrated circuits that have large gate arrays and large routing channels.

### State of the Art:

It is well known to use standardized gate arrays to construct semi-custom integrated circuits. An example of a typical semiconductor integrated circuit or "chip" 15 based upon gate arrays is shown in Figure 1 and is described in United States Patent No. 4,562,453. In this example, the chip 15 has four peripheral blocks 11, 12, 13 and 14 that surround four internal functional gate regions 21, 22, 23 and 24. The spaces between the internal functional gate regions comprise routing channels or "tracks" 31, 32 and 33 for routing wires.

In a gate array chip of the type shown in Figure 1, the peripheral blocks normally are used for input/output functions such as signal level conversion. In the internal functional gate regions, logic gates are regularly arrayed so that various circuits, herein referred to as "macro cells," can be constructed. The macro cells are interconnected by wiring that passes through the routing tracks 31, 32 and 33.

Figure 2A shows a conventional layout of an internal functional gate region or "gate array base" of a gate array chip. More particularly, the drawing depicts a high-density CMOS gate array wherein rows of P-type transistors alternate with rows of N-type transistors. (In the following discussion, a P-type transistor row and an N-type transistor row are together referred to as a placement row.) The transistors are formed in pairs by extending polysilicon gate lines (e.g., line 47) across P-type or N-type diffusion regions (e.g., region 49). A macro cell might be placed, for instance, in the dark outlined region 53 of the gate array base. A typical macro cell is one placement row high and as many rows wide as necessary to realize its required function.

Further in the conventional layout gate array base shown in Figure 2A, every "pair of pairs" -- that is, every four transistors -- is flanked on either side by a substrate connection region (e.g., region 51).

Figure 2B shows a typical example of an AND gate laid out in a macro cell 35 according to the prior art, with the macro cell being a single placement row (i.e., two transistor rows) high. As indicated by the annotations to the drawing, the AND gate is realized from a two input NAND gate -- having inputs A1 and A2, and output X -- which is connected in series with an inverter to produce an output Z. That is, the left-hand side of the macro cell realizes the NAND gate function and the right-hand side realizes the inverter function.

In Figure 2B, the solid shading represents polysilicon (e.g., region 37), the cross-hatching

represents metal (e.g., region 39), and the large dotted-outline rectangular areas (e.g., region 41) represent diffusion regions. The diffusion regions in the upper half of the macro cell are of the P-type, with polysilicon crossing twice above each diffusion region to form four P-type transistors. In the upper left-hand quadrant, the two P-type transistors are connected in parallel by the metal layer so that the transistors share a common output.

In the lower half of the macro cell in Figure 2B, the diffusion regions are of the N-type with polysilicon crossing twice above each diffusion region to form four N-type transistors. More particularly, in the lower left-hand quadrant, two N-type transistors are connected in series with their output being taken to the right of the gate line farthest to the right. The gates of one of the P-type and one of the N-type transistors are joined together to form an input A1, and the gates of the other P-type and other N-type transistors are joined together to form an input A2. The outputs of the parallel P-type combination and the series N-type combination are connected in common by metal to form the output X of the NAND gate.

As also shown in Figure 2B, the macro cell includes contacts between metal and diffusion or polysilicon, represented by square outlines (e.g., region 40). The contacts between metal and a hidden metal layer are represented by a darkened square (e.g., region 43) located in substrate connected regions (e.g., region 45) between the basic cells.

When inputs A1 and A2 are both high during operation of the macro cell of Figure 2B, the P-type transistors are both in the "off" state and the series-

connected N-type transistors are both in the "on" state. This configuration results in a low voltage $V_{SS}$ being passed to the output of the second N-type transistor, thereby causing the output to go low. When either input A1 or A2 is low, at least one of the parallel-connected P-type transistors is "on," with the result that a high voltage $V_{DD}$ is passed through to the common output of the P-type transistors to cause the output to go high. At the same time, at least one of series-connected N-type transistors is off, with the result that the low voltage $V_{SS}$ is not passed through to the output.

On the inverter side of the macro cell of Figure 2B, the output of the NAND gate is connected in common to each of the gates of the two P-type and two N-type transistors. When the output is at voltage $V_{SS}$, the P-type transistors are turned on and, as a result, the high voltage $V_{DD}$ is passed through to the output Z and the two N-type transistors are turned off. When output X is high at $V_{DD}$, the N-type transistors are turned on, with the result that the low voltage $V_{SS}$ is passed through to the output Z and the two P-type transistors are turned off.

One limitation of conventional gate arrays is that the routing area cannot be readily increased. One suggested way to this shortcoming is to run routing channels parallel to the transistors, thereby forming a column macro cell. This solution, however, constrains the macro cell sizes to be of fixed width and of a height that is a multiple of a large number of routing tracks (for example, eight). Thus, in this suggested solution, flexibility in routing channel size was gained at the expense of reduced flexibility in sizing macro cells.

Another suggested solution to the above-described shortcoming was to use field isolation (instead of gate isolation) and to separate P-type and N-type transistor gates. With the gates separated, a routing channel can be as small as either the N-type or P-type transistors. With the P-type and N-type gates connected according to the gate isolation technique, by contrast, a routing channel must be as high as the sum of the heights of the P-type and N-type transistors.

Even in field isolated designs, however, the commonly-used routing channel size has been approximately the same as the height of one P-type and N-type transistor. For large gate arrays, the resulting routing channel size is not large enough if the transistors are small. If the transistors are made larger, the routing channel size is less adjustable, since the minimum increment is the height of a P-type or N-type transistor. Large transistors also have larger gate capacitances, a disadvantage in many circuits.

## SUMMARY OF THE INVENTION

The present invention, generally speaking, provides for realizing large semi-custom integrated circuits having large gate arrays and large routing channels while maintaining routing efficiency such that no more than fifty percent of the transistors of the gate array are routed over. In the preferred embodiment of the present invention, a gate array has multiple transistor rows, each transistor row containing multiple transistors all of a given type, alternate transistor rows containing transistors of opposite types, each transistor row being five or more routing tracks high in a column direction; and a

plurality of functional units, each at least twenty routing tracks high in a column direction. In effect, small transistors are used to create tall macro cells by putting more than two rows of transistors in a macro cell. For example, a macro cell can include four rows of transistors with the rows alternating between P-type and N-type transistors and with the number of rows increasing as the size of design increases. Preferably, a macro cell uses an even number of rows such that macro cells can abut if no routing channel is required.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be further understood with reference to the following description in conjunction with the appended drawings, wherein like elements are provided with the same reference numerals. In the drawings:

Figure 1 is a plan view of a gate array chip according to the prior art;

Figure 2A is a plan view of a gate array base according to the prior art;

Figure 2B is a plan view of a macro cell according to the prior art;

Figure 3 is the plan view of an AND gate macro cell according to the present invention; and

Figure 4 is a plan view of the gate array base according to the present invention showing a typical arrangement of a placement row and a routing channel.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 3 shows tall macro cells created from small transistors to realize the AND function by providing a placement row that is four transistor rows high as compared to the two transistor rows of Figure 2B. Also, the transistor rows in Figure 3 are only half as high as the transistor rows of Figure 2B, with the result that the overall height of the placement row is the same.

Using current technology, the transistor rows of Figures 2B and 3 can each be sixteen microns high (five routing tracks at a routing pitch of 3.2 microns).

By using macro cells such as shown in Figure 3 and by alternating routing channels and cell placement rows as shown in Figure 4, large routing channels (e.g., twenty routing tracks high) can be achieved without routing over more than fifty percent of the transistors. If instead macro cells were designed using only two small transistor rows, for example, a routing channel of more than ten tracks would require more than two rows, with the result that more than half the area of the combined area of the macro cell and the routing channel would be dedicated to the routing channel.

In practice, not every routing channel on a gate array need be the same size. Using macro cells such as shown in Figure 3, for instance, the size of the routing channel can be increased in increments of five routing tracks (which is the size of a transistor row). Routing channels may therefore be of a size "5n"

routing tracks where "n" is an integer including 0, resulting in considerable routing flexibility.

Many types of circuits are better implemented using small transistors as in the macro cell of Figure 3. For example, speed improvements can be achieved by, wherever practicable, having the inputs of the macro cell drive only a single small transistor pair while the outputs of the macro cell drive more than one small transistor pair. Thus, the drive capability of a macro cell can be increased without increasing its input load. In Figure 3, for example, each of the inputs A1 and A2 is used to drive one P-type and one N-type transistor whereas the output Z is driven by two P-type and two N-type transistors.

In the gate array base in Figure 4, using macro cells four transistor rows high as exemplified by the macro cell of Figure 3, alternate placement rows may be used for cell placement and routing, respectively, as in the prior art, but the resulting routing channel is now twenty routing tracks high, sufficient for routing of large, dense gate arrays. Routing channels nevertheless do not occupy more than 50% of the gate array base. Furthermore, if a routing channel more or less than twenty routing tracks high is needed, the routing channel may be easily increased in increments of five routing tracks. Also, because the transistors are made small, versatility is achieved since small transistors are available for circuits requiring them, and small transistors may be interconnected as necessary to form large transistors to create large drive macro cells wherever necessary.

The foregoing has described the principles, preferred embodiments and modes of operation of the

present invention. However, the invention should not be construed as limited to the particular embodiments discussed. Instead, the above-described embodiments should be regarded as illustrative rather than restrictive, and it should be appreciated that variations may be made in those embodiments by workers skilled in the art without departing from the scope of the present invention as defined by the following claims.

WHAT IS CLAIMED IS:

1. A circuit comprising:

a gate array having multiple transistor rows, each transistor row containing multiple transistors of a given type, alternate transistor rows containing transistors of opposite types;

a plurality of functional units encompassing at least four of the transistor rows; and

a routing area formed above unconnected transistors in transistor rows different from the transistor rows encompassed by the functional units and containing interconnections between the functional units, the routing area encompassing a number of transistor rows from zero to four or more.

2. A circuit comprising:

a gate array having multiple transistor rows, each transistor row containing multiple transistors of a given type, alternate transistor rows containing transistors of opposite types;

a plurality of functional units encompassing at least four of the transistor rows; and

a routing area containing interconnections between the functional units and formed in an area that would otherwise contain a number of transistor rows from zero to four or more.

3. A method of laying out a circuit having as part thereof a gate array with multiple transistor rows, each transistor row containing multiple transistors of a given type, alternate transistor rows containing transistors of opposite types, comprising the steps of:

defining a plurality of functional units encompassing at least four of the transistor rows; and

reserving a routing area for interconnections between the functional units in an area that would otherwise contain a number of transistor rows from zero to four or more.

4. A circuit comprising:

a gate array having multiple transistor rows, each transistor row containing multiple transistors of a given type, alternate transistor rows containing transistors of opposite types;

a plurality of functional units encompassing more than two of the transistor rows; and

a routing area formed above unconnected transistors in transistor rows different from the transistor rows encompassed by the functional units and containing interconnections between the functional units, the routing area encompassing a number of transistor rows from zero to four or more.

5. A circuit comprising:

a gate array having multiple transistor rows, each transistor row containing multiple transistors all of a given type, alternate transistor rows containing transistors of opposite types, each transistor row being five or more routing tracks high in a column direction; and

a plurality of functional units, each at least twenty routing tracks high in a column direction, interconnected to form the circuit.

6. The circuit of Claim 5 further comprising a routing area containing interconnections between the functional units and formed in an area that would otherwise contain an integral number of transistor rows.

7. The circuit of Claim 6 wherein at least one input of at least one of the functional units drives only a single pair of the transistors and at least one output of the one of the functional units is driven by more than one pair of the transistors.

8. A method of laying out a circuit having as part thereof a gate array with multiple transistor rows, each transistor row containing multiple transistors all of a given type, alternate transistor rows containing transistors of opposite types, each transistor row being five or more routing tracks high in a column direction, the method comprising the steps of:

defining a plurality of functional units each at least twenty routing tracks high in a column direction; and

reserving a routing area for interconnections between the functional units and having an area equivalent to that of an integral number of the transistor rows.

9. The method of Claim 8 wherein at least one of the functional units has at least one input driving only a single pair of the transistors and at least one output is driven by more than one pair of the transistors.

10. A digital logic macro cell having at least one input and at least one output and performing a digital logic function, comprising at least eight transistors each having a gate electrode and a source/drain electrode and arrayed in at least four rows in a direction of the gate electrodes with the gate electrodes and the source drain electrodes,

respectively, of each of the at least eight transistors being virtually parallel.

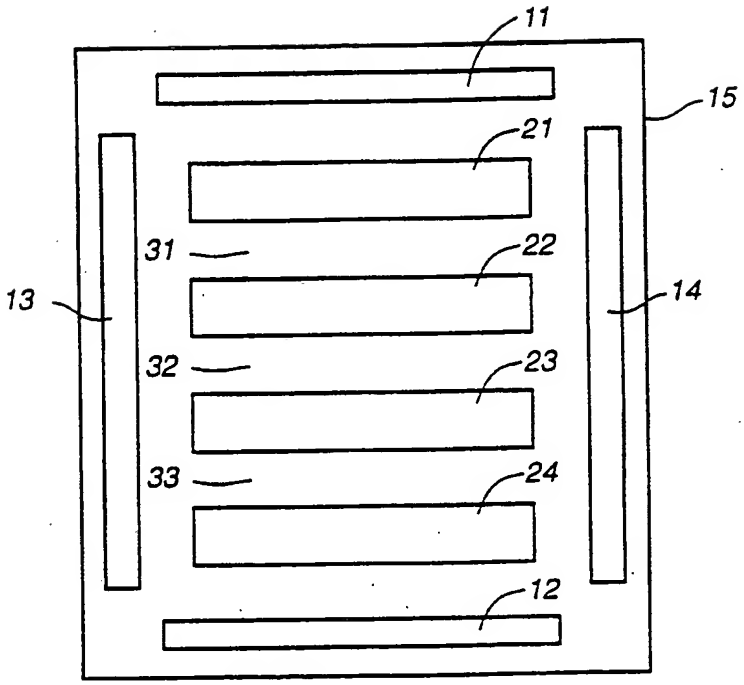


FIG._1
(PRIOR ART)

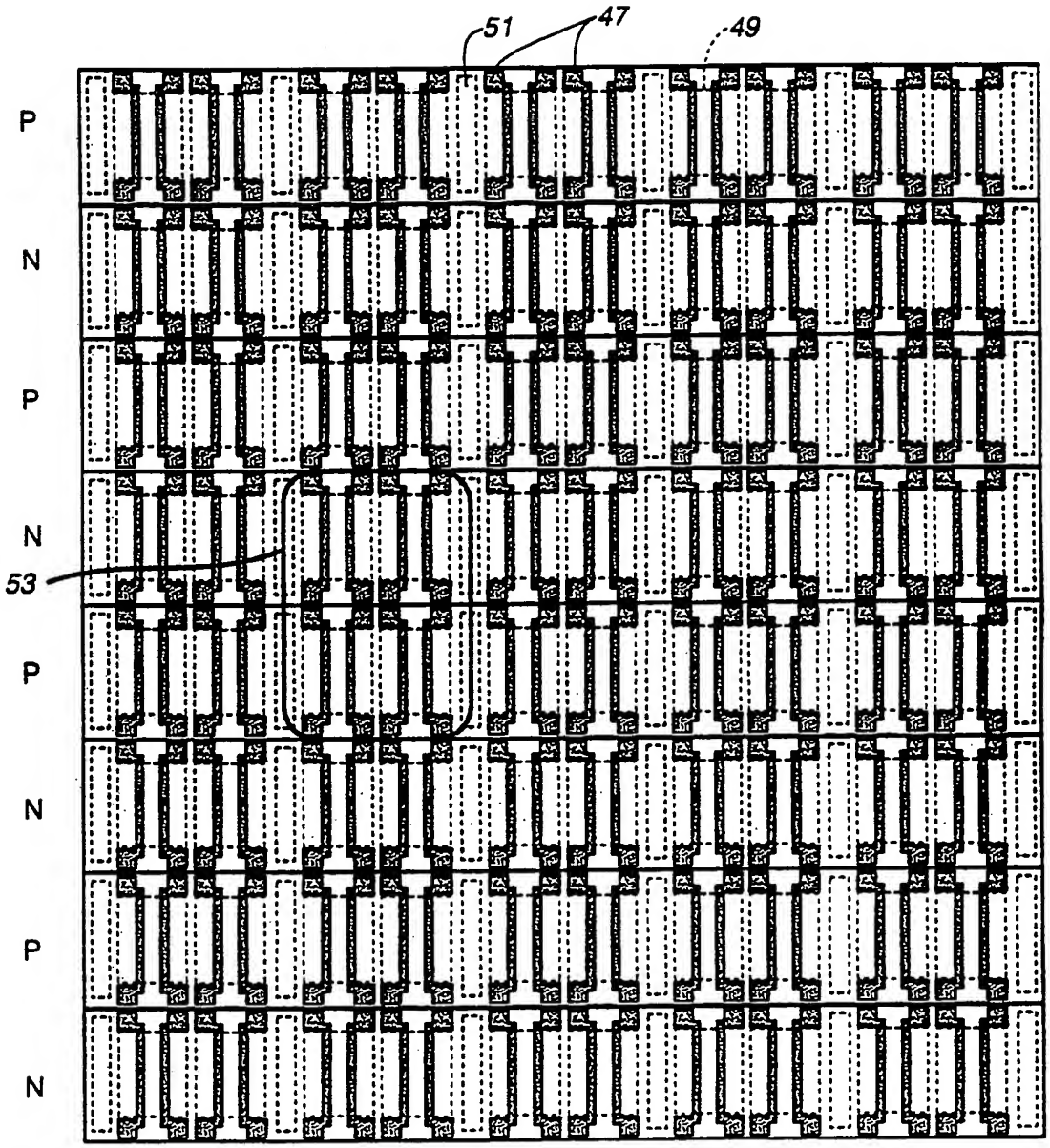


FIG._2A
(PRIOR ART)

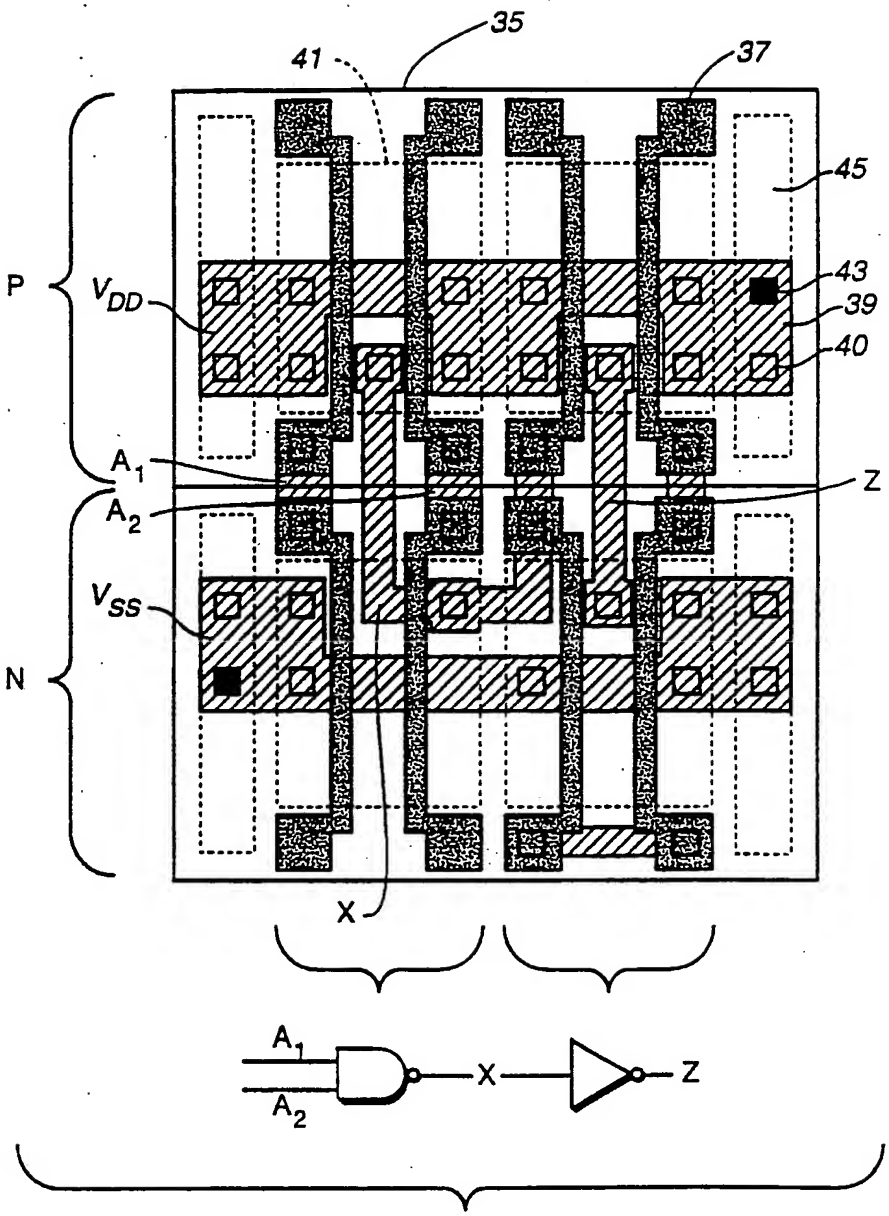


FIG._2B
(PRIOR ART)

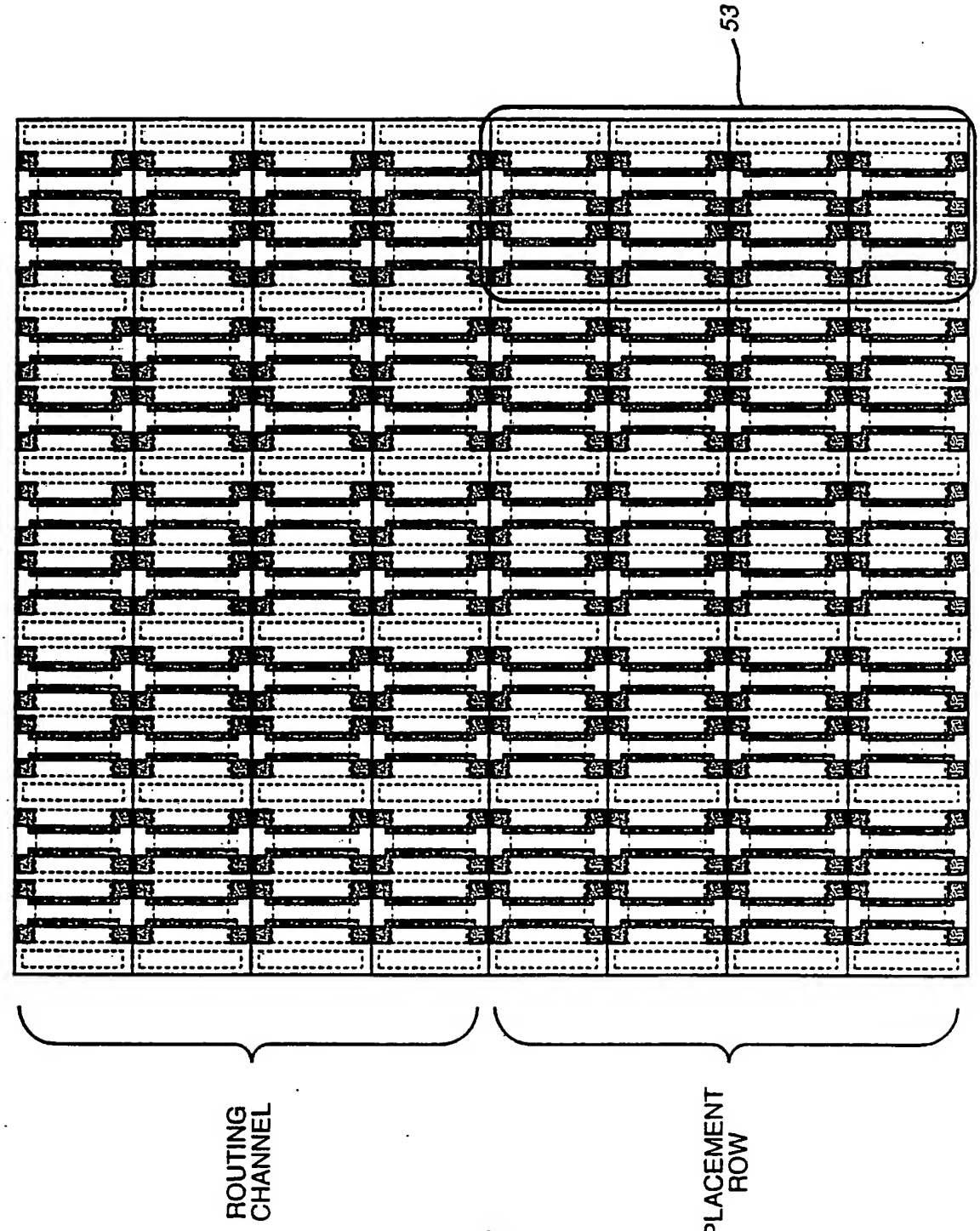


FIG._4

# INTERNATIONAL SEARCH REPORT

PCT/US92/09523

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(5) :H01L 27/10, 27/15
US CL :257/202,203,204,206,207,208,209,210,211
According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/202,203,204,206,207,208,209,210,211

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

none

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>Y | JP,A G2-249450 (USUI) 30 October 1987 see the abstract and figures 1-13. | 1-4<br>5-9 |
| X<br>Y | JP, 59-11670 (Takada) 21 January 1984 See the abstract and figures 1-5. | 1-4<br>5-9 |
| X<br>Y | JP, 59-63743 (Otani) 11 April 1984 See the abstract and figures 1-3. | 1-4<br>5-9 |
| X<br>Y | JP, 1-125846 (Mizuno) 18 May 1989 See the abstract and figures 1-9. | 1-4<br>5-9 |
| X | US,A, 4,791,474 (Sugiura et al.) 13 December 1988. | 10 |

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/09523

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>Y | US,A, 4,611,236 (Sato) 9 September 1986 See figures 5 to 12. | 10<br>1-9 |
| X | US,A, 4,661,815 (Takayama et al.) 28 April 1987 See figure 11. | 10 |

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/09523

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

Group I, claims 1,2 and 4-7, drawn to a gate array circuit, classified in class 257, subclass 204.

Group II, claims 3,8, and 9, drawn to method of laying out a circuit, classifed in class 437, subclass 946.

Group III, claim 10, drawn to a digital logic macro cell, classified in class 307, subclass 440.

and it considers that the international application does not comply with requirements of unity of invention (Rules 13.1, 13.2, and 13.3) for the reasons indicated below:

Group I and II are related as product and a method of laying out that product, the product, as claimed can be laid out by different methods, e.g. reserving a routing area before defining a plurality of functional units.

Group I and III are independent from each other. The digital logic macro cell does not have the routing area as defined in the claims of Group I.